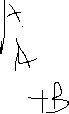
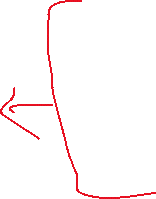
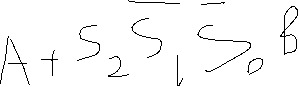
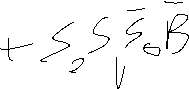
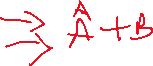
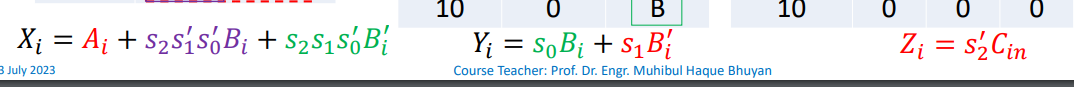
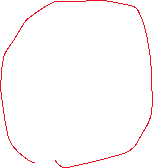
A screenshot of a computer

Description automatically generated



A diagram of a circuit

Description automatically generated



A close-up of a paper

Description automatically generated



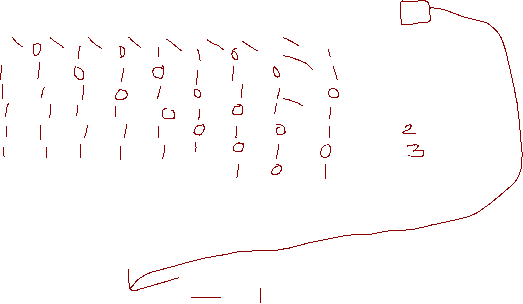
A diagram of a multiplexer

Description automatically generated



A screenshot of a chart

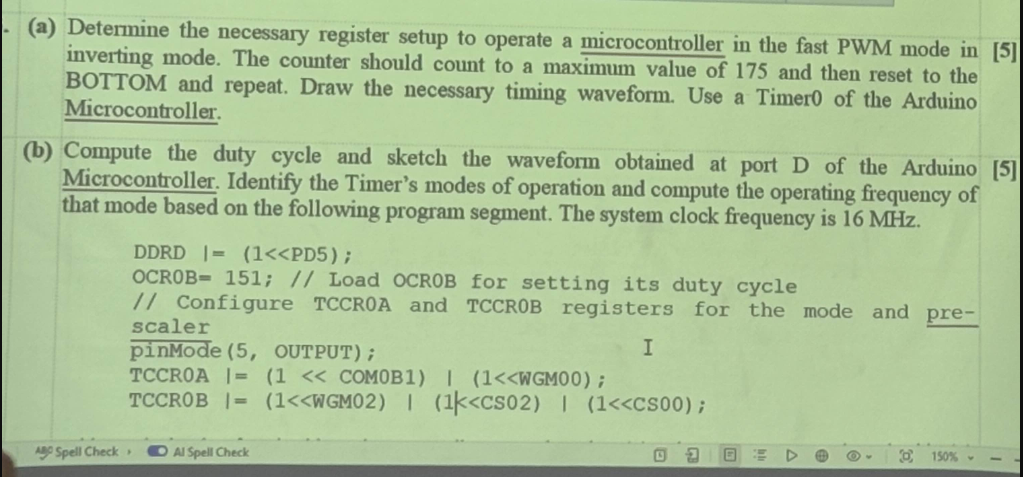
Description automatically generated



A diagram of a flowchart

Description automatically generated

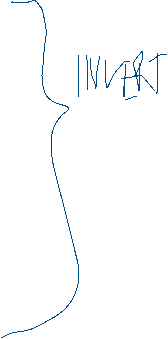




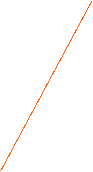
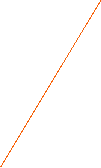
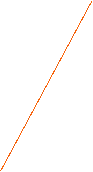
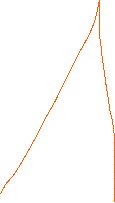


A close up of a paper

Description automatically generated



**b)** Given, here, Timer0 is used. Since WGM02:1, WGM01:0 bit so WGM00:1 bit so it will be in 101, it will operate in the Phase correct PWM mode 5. Since COM0B1:1 bits are set to 10, it will produce a **non-inverted PWM** signal at port D. Since CS bits are set to 101, the pre-scaler value is 1024. The PWM frequency of Output for the Phase correct PWM Mode is:



System clock frequency, fclk 16 MHz = 16 ×106 Hz

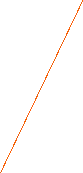
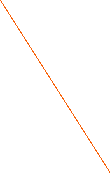
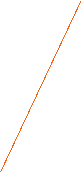
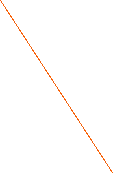
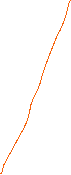
OCR0B = 151

Frequency = *fPWM* = = = 51.73 ~ 52 Hz

Duty cycle for **non-inverted PWM.**

Duty Cycle for, OCR0B = => D = = = 0.6 \* 100 = 60%

****



**4)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **D** | **F** | **Cin** | **H** | **hex** |
| **010** | **010** | **011** | **011** | **0** | **110** | **49B6h** |
| **001** | **100** | **011** | **001** | **1** | **000** |  |
| **110** | **000** | **000** | **011** | **0** | **000** |  |
| **100** | **010** | **011** | **010** | **1** | **000** |  |
| **010** | **100** | **000** | **101** | **0** | **000** |  |
|  |  |  |  |  |  |  |

**(010 010 011 011 0 110)2  = (49B6)16**

**b) UBBRN = 2745**

**f = 16 \*10^6**

**baud rate = (16\*10^6)/(2\*(2745+1) = 2913.32 = 2914**

**baud error rate = (2400-2914)/2400 = -21% > +-2%**